IN THE CLAIMS:

1. (Currently Amended) A data transferring apparatus for transferring liquid ejection data, comprising:

a bus system, which comprises two independent bus systems of a system bus and a local bus;

a local memory coupled to said local bus in order to be able to transfer data to said local bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a receiving buffer unit comprising a main memory for storing liquid ejection data compressed to be capable of line development;

a head controlling unit comprising a register of a liquid ejecting head;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development, wherein said decode unit is coupled to said system bus and local bus in order to transfer data therebetween;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said receiving buffer unit comprises:

a command storing register which is accessible from said system bus,

a header analyzing unit for analyzing a header of said liquid ejection controlling data,

a command separating unit for separating a command from said liquid ejection controlling data according to [[said]] an analysis result of said header analyzing unit and storing said command into said command storing register, and

a data transfer controlling unit for storing liquid ejection controlling data, from which said command is separated, into said main memory.

2. (Original) A data transferring apparatus as claimed in claim 1, wherein

said receiving buffer unit further comprises a data separating unit for separating said liquid ejection controlling data stored in said main memory into a remote command and liquid ejection data compressed to be capable of line development,

said remote command is processed by a microprocessor coupled to said system bus, and

said liquid ejection data compressed to be capable of line development is transferred to said decode unit.

3. (Original) A data transferring apparatus for transferring liquid ejection data, comprising:

a bus system, which comprises two independent bus systems of a system bus and a local bus;

transfer data to said local bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a receiving buffer unit comprising a main memory for storing liquid ejection data compressed to be capable of line development;

a head controlling unit comprising a register of a liquid ejecting head;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development, wherein said decode unit is coupled to said system bus and local bus in order to transfer data therebetween;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said receiving buffer unit comprises:

a data transfer controlling unit for storing liquid ejection controlling data received by said interface unit into said main memory, and

a data separating unit for separating said liquid ejection controlling data stored in said main memory into a command and liquid ejection data compressed to be capable of line development,

wherein said command is processed by a microprocessor coupled to said system bus, and

said liquid ejection data compressed to be capable of line development is transferred to said decode unit.

4. (Original) A data transferring apparatus as claimed in claim 3, wherein said decode unit further comprises:

a line buffer for storing said liquid ejection data developed by said decode circuit by word unit, and

a DMA transferring unit for performing DMA transfer on said liquid ejection data compressed to be capable of line development to said decode circuit from said main memory, performing DMA transfer on said liquid ejection data developed in said line buffer to said local memory by word unit, and performing sequential DMA transfer on said developed liquid ejection data stored in said local memory to said register of said liquid ejecting head.

5. (Original) A data transferring apparatus as claimed in claim 4, wherein said line buffer further comprises two (2) faces of buffer areas for storing developed data of predetermined words, said liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas, while said liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when said developed data of predetermined words is accumulated, and DMA transfer to said local memory is performed per predetermined words with respect to said developed data when said developed data of predetermined words is accumulated.

6. (Original) A data transferring apparatus as claimed in claim 5, wherein one (1) ASIC comprises said interface unit, said receiving buffer unit, said decode unit, said head controlling unit and said first, second and third dedicated buses.

7. (Original) A data transferring apparatus as claimed in claim 6, wherein said data transfer to said local memory from said decode unit and to said register of said liquid ejecting head from said local memory on said local bus is performed by burst transfer.

8. (Original) A data transferring apparatus as claimed in claim 7, wherein said compressed liquid ejection data is run length compression data, and said decode circuit can perform hardware development on run length compression data.

9. (Original) A data transferring apparatus as claimed in claim 8, wherein said decode unit further comprises a means for storing uncompressed liquid ejection data, which is DMA-

transferred from said main memory, into said line buffer without hardware development by said decode circuit.

10. (Currently Amended) A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data, said data transferring apparatus comprising:

a bus system, which comprises two independent bus systems of a system bus and a local bus;

a local memory coupled to said local bus in order to be able to transfer data to said local bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a receiving buffer unit comprising a main memory for storing liquid ejection data compressed to be capable of line development;

a head controlling unit comprising a register of a liquid ejecting head;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development, wherein said decode unit is coupled to said system bus and local bus in order to transfer data therebetween;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said receiving buffer unit comprises:

a command storing register which is accessible from said system bus,

a header analyzing unit for analyzing a header of said liquid ejection controlling data,

a command separating unit for separating a command from said liquid ejection controlling data according to [[said]] an analysis result of said header analyzing unit and storing said command into said command storing register, and

a data transfer controlling unit for storing liquid ejection controlling data, from which said command is separated, into said main memory.

11. (Original) A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data, said data transferring apparatus comprising:

a bus system, which comprises two independent bus systems of a system bus and a local bus;

a local memory coupled to said local bus in order to be able to transfer data to said local bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a receiving buffer unit comprising a main memory for storing liquid ejection data compressed to be capable of line development;

a head controlling unit comprising a register of a liquid ejecting head;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development, wherein said decode unit is coupled to said system bus and local bus in order to transfer data therebetween;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said receiving buffer unit comprises:

a data transfer controlling unit for storing liquid ejection controlling data received by said interface unit into said main memory, and

a data separating unit for separating said liquid ejection controlling data stored in said main memory into a command and liquid ejection data compressed to be capable of line development,

wherein said command is processed by a microprocessor coupled to said system bus, and

said liquid ejection data compressed to be capable of line development is transferred to said decode unit.

12. (Currently Amended) A data transferring apparatus for transferring liquid ejection data, comprising:

a bus system, which comprises two independent bus systems of a system bus and a local bus;

a local memory coupled to said local bus in order to be able to transfer data to said local bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a receiving buffer unit comprising a main memory for storing liquid ejection data compressed to be capable of line development;

a head controlling unit comprising a register of a liquid ejecting head;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development, wherein said decode unit is coupled to said system bus and local bus in order to transfer data therebetween;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said interface unit comprises:

a command storing register which is accessible from said system bus,

a header analyzing unit for analyzing a header of said liquid ejection controlling data,

a command separating unit for separating a command from said liquid ejection controlling data according to [[said]] an analysis result of said header analyzing unit and storing said command into said command storing register, and

a data transfer controlling unit for storing liquid ejection controlling data, from which said command is separated, into said main memory.

13. (Original) A data transferring apparatus as claimed in claim 12, wherein

said receiving buffer unit further comprises a data separating unit for separating said liquid ejection controlling data stored in said main memory into a remote command and liquid ejection data compressed to be capable of line development,

said remote command is processed by a microprocessor coupled to said system bus, and

said liquid ejection data compressed to be capable of line development is transferred to said decode unit.

14. (Original) A data transferring apparatus as claimed in claim 13, wherein said decode unit further comprises:

a line buffer for storing said liquid ejection data developed by said decode circuit by word unit, and

a DMA transferring unit for performing DMA transfer on said liquid ejection data compressed to be capable of line development to said decode circuit from said main memory, performing DMA transfer on said liquid ejection data developed in said line buffer to said local memory by word unit, and performing sequential DMA transfer on said developed liquid ejection data stored in said local memory to said register of said liquid ejecting head.

15. (Original) A data transferring apparatus as claimed in claim 14, wherein said line buffer further comprises two (2) faces of buffer areas for storing developed data of predetermined words, said liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas, while said liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when said developed data of predetermined words is accumulated, and DMA transfer to said local memory is performed per predetermined words with respect to said developed data when said developed data of predetermined words is accumulated.

16. (Original) A data transferring apparatus as claimed in claim 15, wherein one (1) ASIC comprises said interface unit, said receiving buffer unit, said decode unit, said head controlling unit and said first, second and third dedicated buses.

17. (Original) A data transferring apparatus as claimed in claim 16, wherein said data transfer to said local memory from said decode unit and to said register of said liquid ejecting head from said local memory on said local bus is performed by burst transfer.

18. (Original) A data transferring apparatus as claimed in claim 17, wherein said compressed liquid ejection data is run length compression data, and said decode circuit can perform hardware development on run length compression data.

19. (Original) A data transferring apparatus as claimed in claim 18, wherein said

decode unit further comprises a means for storing uncompressed liquid ejection data, which is DMA-transferred from said main memory, into said line buffer without hardware development by said decode circuit.

20. (Original) A liquid ejecting apparatus comprising a data transferring apparatus for transferring liquid ejection data, said data transferring apparatus comprising:

a bus system, which comprises two independent bus systems of a system bus and a local bus;

a local memory coupled to said local bus in order to be able to transfer data to said local bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a receiving buffer unit comprising a main memory for storing liquid ejection data compressed to be capable of line development;

a head controlling unit comprising a register of a liquid ejecting head;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development, wherein said decode unit is coupled to said system bus and local bus in order to transfer data therebetween;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said interface unit comprises:

a command storing register which is accessible from said system bus,

a header analyzing unit for analyzing a header of said liquid ejection controlling data,

a command separating unit for separating a command from said liquid ejection controlling data according to said analysis result of said header analyzing unit and storing said command into said command storing register, and

a data transfer controlling unit for storing liquid ejection controlling data, from which said command is separated, into said main memory.